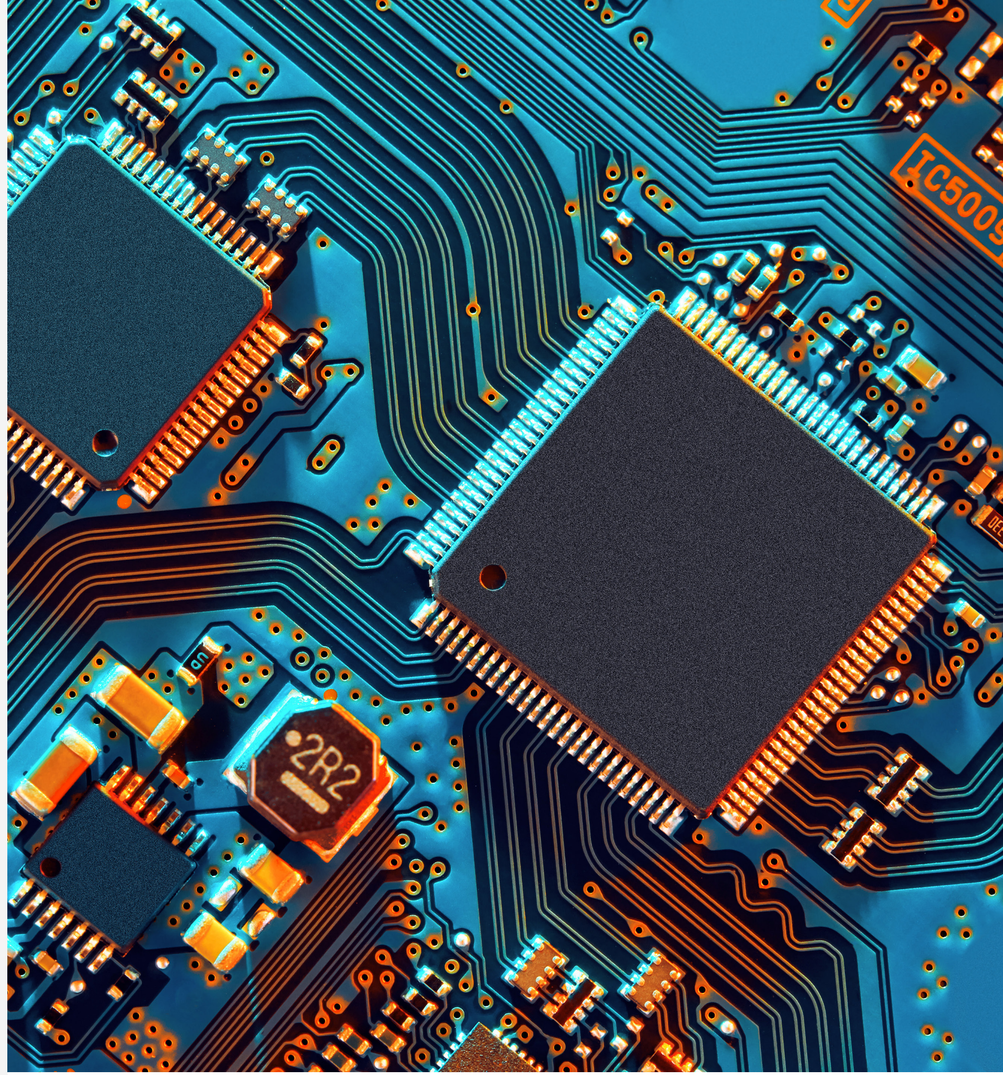
Enabling Compact, Efficient Designs with High Voltage CoolSiC™ Discretes



Mighty Guides

Sponsored by

Infineon | MOUSER ELECTRONICS

Table of Contents

Mighty Guides

Introduction

The power electronics industry stands at a crucial inflection point. As industrial applications demand higher efficiency, greater power density, and reduced costs, traditional silicon-based solutions increasingly fall short. This comprehensive guide explores how Infineon's CoolSiC™ technology portfolio directly addresses these issues, offering engineers the tools they need to develop next-generation power systems.

Today's industrial applications — from solar inverters and energy storage systems to EV charging infrastructure — are boosting DC link voltages to unprecedented levels, reaching up to 1500V. This trend signals a fundamental change: higher voltages enable greater power ratings with significantly reduced losses, but they also require semiconductors capable of reliably handling these extreme conditions.

Infineon's CoolSiC™ technology portfolio provides 2000V SiC devices with an impressive RDS(on) range, from 100 milliohms down to just 7 milliohms. Built on an innovative trench design, these devices deliver exceptional gate oxide reliability, immunity to parasitic turn-on, and the ability to operate at 0V gate-source voltage, greatly simplifying system design.

This guide explores four key areas to accelerate your power design development:

Technology Evolution: Discover the strategic step from Generation 1 to Generation 2, where significant improvements in switching efficiency, thermal management, and package design lead to measurable performance gains.

Enhanced Performance: Learn about our innovative .XT interconnection technology, which achieves 30% better thermal resistance while providing superior electrical performance.

Smart Packaging Solutions: Explore the game-changing topside-cooled Q-DPAK design that eliminates the traditional trade-off between thermal performance and manufacturing efficiency.

Design Support: Access comprehensive development resources, including advanced simulation tools and validated reference designs that help streamline your project timeline.

Whether you're designing solar inverters, energy storage systems, or industrial drives, this guide demonstrates how CoolSiC™ technology can transform your approach to power electronics—providing the performance, reliability, and design flexibility your applications demand.

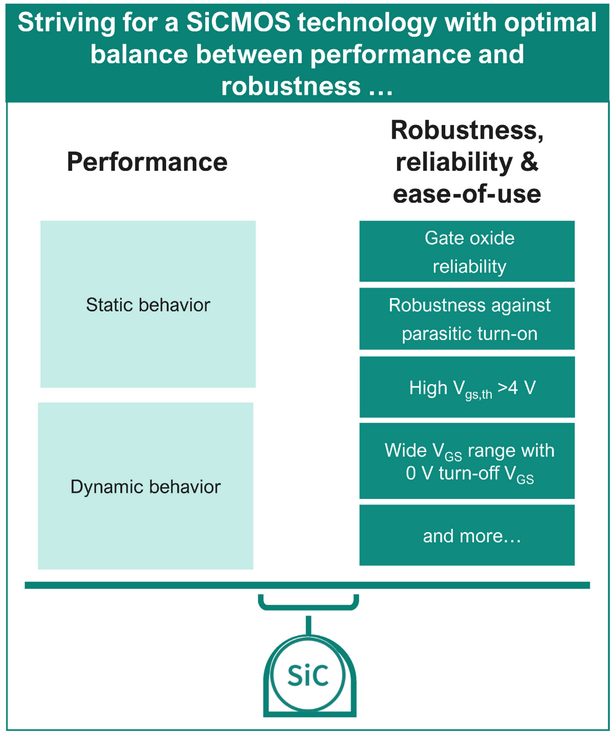
Chapter 1

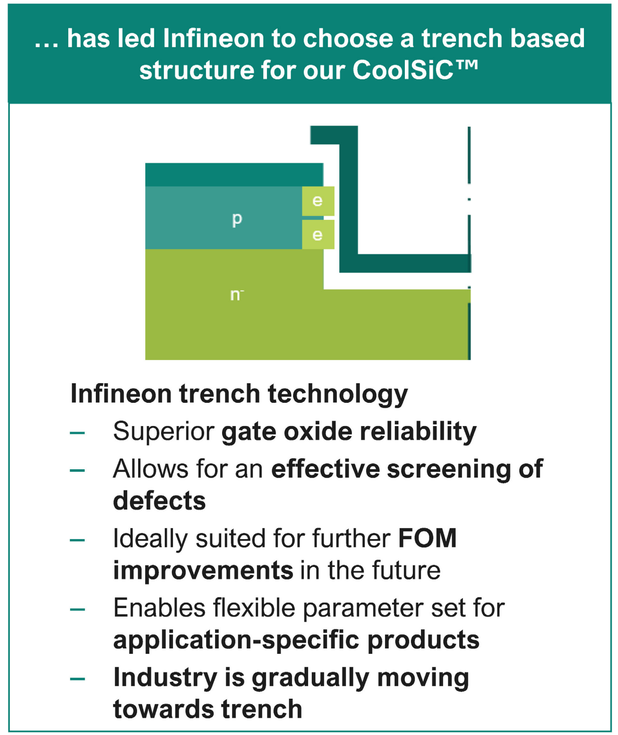
Technology Overview and Evolution of the 1200 V CoolSiC™ Technology

Trench Design and Technology Foundation

Central to Infineon's CoolSiC™ technology is its innovative trench design. This architecture solves a long-standing challenge for power semiconductor designers—balancing performance, robustness, and reliability. By maximizing efficiency while ensuring device longevity, the trench design sets CoolSiC™ apart in the silicon carbide industry.

What makes this design notable is its gate oxide reliability. Infineon's CoolSiC™ trench design achieves gate oxide reliability, which directly improves performance in real-world applications. This means devices that not only perform better but also last longer under demanding conditions.





Additionally, the technology addresses a common challenge in power electronics: parasitic turn-on. CoolSiC™ devices are resistant to these unwanted switching events because of their higher gate-source threshold voltage as well as the improved ratio of CGD and CDS capacitances. This allows engineers to operate the device at a gate-source voltage turn-off of 0 volts, removing the need for negative gate voltages and making system design and integration easier.

Technology Evolution of CoolSiC™ from G1 to G2 Industrial Lead Type

Establishing the Foundation

The CoolSiC™ journey began with M1 technology, showing that a trench-based design could deliver both high performance and dependability. Not only did this first generation meet expectations, but it also set new standards with its strong short-circuit capacity and a carefully optimized gate oxide for a Vgs(on) of 15V at the rated RDS(on).

Additionally, M1 introduced dV/dt controllability, enabling precise management of switching behavior. Coupled with its resistance to parasitic turn-on, these features created a reliable foundation that would shape the platform's future.

Pushing Performance Boundaries

While M1 established reliability, the market demanded even higher performance. The M1H technology responded to this challenge by building on all of M1's benefits while pushing a boundary: the gate oxide optimization. By engineering the gate oxide to operate reliably at Vgs of 18V instead of 15V, M1H unlocked additional performance improvements.

This 3-volt increase may seem modest, but it represents a significant advance in the technology's capabilities, enabling lower losses and higher efficiency while preserving the robustness that contributed to M1's success.

M2H: Achieving Cost-Performance Improvement

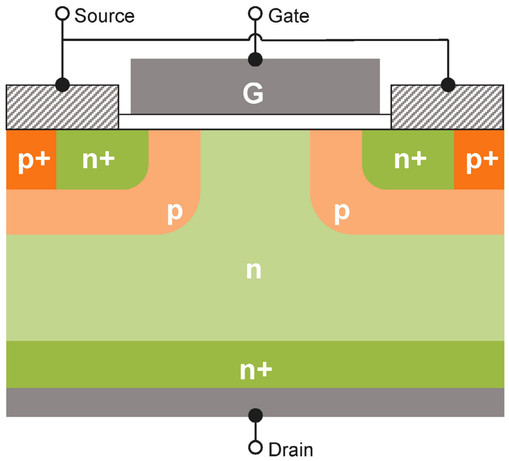
With proven performance and reliability, the next challenge was clear: making the technology accessible for broader market adoption. M2H technology directly addresses this by implementing strategic optimizations aimed at improving cost-performance.

By reducing cell pitch and refining the doping profile, M2H boosts device performance in two key areas: switching characteristics and thermal efficiency. These improvements are achieved without sacrificing robustness or reliability, which remain consistent with earlier versions.

A Platform Built for Progress

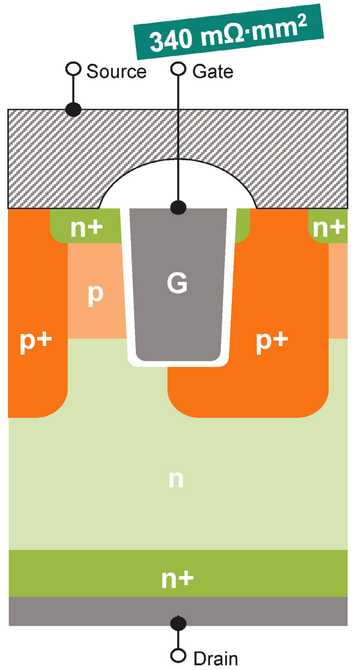
The evolution of CoolSiC™ technology follows a clear strategy: build a solid foundation, improve performance where it matters most, and refine for practical application. Through this structured approach, Infineon has developed not just a single product but a platform that continuously adapts to market needs, always keeping the core benefits of the trench design while enhancing performance and value.

„Generation 0“



Features:
Less complex processing but limited channel width/cell pitch
Reliability impossible to merge with all performance requirements
Mostly thin GOX, low $V_{gs(th)}$ and high V_{GSon} for acceptable R_{DSon}·A ➔ reliability risk
Limited control for essential parameters like $V_{gs(th)}$

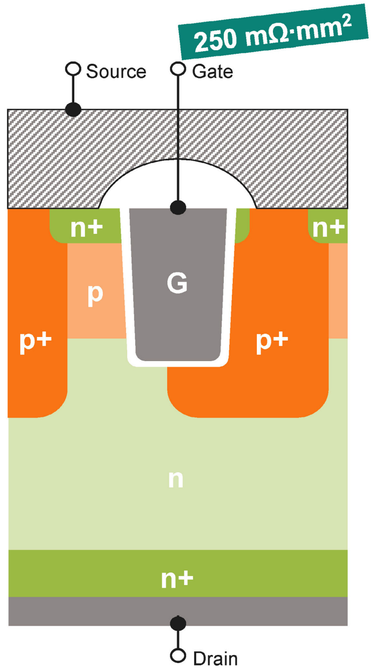
CoolSiC™ M1



Features:
High performance and high reliability enabled by trench concept

Short circuit rugged (for 1200V)
Designed for V_{GSon} = +15 V (for rated Rdson)
dv/dt controllable and rugged against PTO (possible due to high $V_{GS(th)}$ and optimized capacitances)

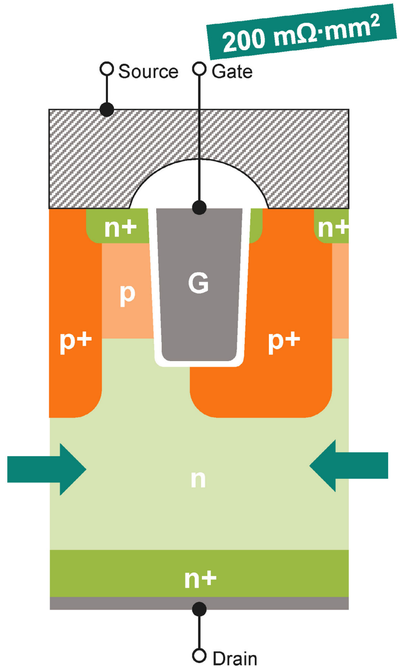
CoolSiC™ M1H



Features: all M1 benefits plus :
Performance gain enabled by V_{GSon} = +18V (GOX optimization and smaller process tunings)

Full utilization of Vgs window independent of f_{sw}, Reduced switching losses
Reduced conduction losses
SC ruggedness is maintained at Vgs = 15V

CoolSiC™ M2



Features: all M1H benefits except SC ruggedness ➔ new 2µs for Vgs=15V
Cost-performance improvement by cell pitch reduction, and doping profile optimization
Lower total losses in all operating modes
.XT interconnect technology for IND products
Further improved PTO ruggedness,
$V_{gs(th)}$ spread reduction

Chapter 2

Electrical and Thermal Performance of 1200 V CoolSiC™ MOSFET G2 in TO-247-4HC Package

Generation 2 Portfolio Overview

The transition from Generation 1 to Generation 2 CoolSiC™ devices in the TO247 4-pin package marks a significant advancement in power semiconductor technology. This chapter discusses how Generation 2 builds on its predecessor's foundation to deliver improved performance in several areas.

Generation 1 started with standard soft soldering in a conventional package and later adopted .XT interconnection technology with an optimized pinout featuring thinner gate and Kelvin pins. Generation 2 enhances these features further by adding a wider creepage distance of 9mm and expanding the RDS(on) range from 78 milliohms to just 7 milliohms. It also provides a 15% better price-performance ratio while reducing switching losses, improving thermal resistance, and increasing gate-source voltage capability.

Performance Enhancements

At the core of Generation 2's progress is its optimized switching performance. The technology shows a 25% reduction in switching losses compared to other SiC technologies, which directly results in lower overall power losses and higher system efficiency.

This improvement is evident when analyzing measured switching transients. Under identical operating conditions—same current, voltage, and temperature—and with dV/dt fixed by adjusting external gate resistance, Generation 2 demonstrates faster di/dt transients than Generation 1, leading to reduced turn-on (Eon) energy losses. Additionally, when operated at the same external gate resistance, Generation 2 achieves both faster di/dt and dV/dt transients, significantly reducing switching energy losses.

Thermal Excellence Through .XT Technology

The switching improvements are enhanced by superior thermal management through .XT interconnection technology. This die attach method uses diffusion soldering, in which the die bonds to the leadframe under high temperature and pressure, eliminating the traditional solder joint. While standard soldering creates a thick interfacial layer, .XT technology removes this thermal bottleneck.

The results are impressive:

- 30% increase in thermal resistance compared to Generation 1 standard soft-solder devices
- 7% increase even against Generation 1 diffusion-solder devices
- 15% lower RTH for devices with similar RDS(on) in the same package

These thermal improvements, combined with the switching loss reduction, provide three main benefits:

- 11% higher output current capacity compared to Generation 1
- 10°C cooler operation when directly replacing Generation 1 in existing systems
- Up to 50% higher switching frequency, allowing for more compact designs

Portfolio Range and Flexibility

Generation 2's expanded portfolio addresses diverse application needs with RDS(on) values:

- TO247: 7 to 78 milliohms (lowest available on the market)
- Q-DPAK: Down to 4 milliohms
- D²PAK: Down to 8 milliohms

This range, combined with the guaranteed maximum RDS(on) at high temperatures specified in the datasheet, simplifies system design by providing appropriate safety margins.

Revolutionary Package Design: Engineering for Real-World Applications

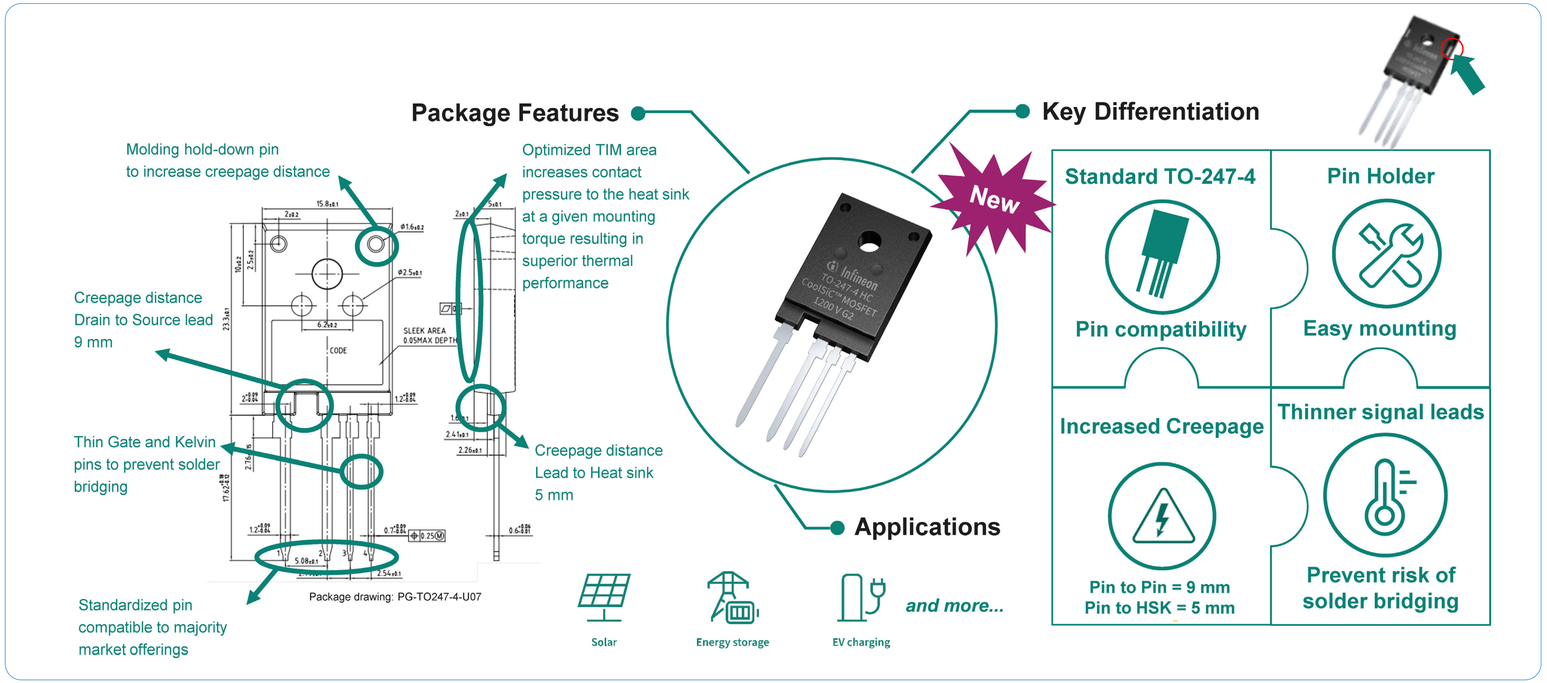
The TO247 4-pin high creepage package maintains compatibility with existing standards while adding new features. It remains pin-to-pin compatible with standard TO247 4-pin packages from any manufacturer, allowing for easy replacement without board modifications. However, several innovations within this familiar footprint improve reliability and simplify use.

The Trouser Design: Extending Creepage Distances

A unique "trouser design" extends the mold body along the leads, creating steps on both the front and back sides. Paired with strategic grooves, this design results in:

Pin-to-pin creepage distance: 9mm

Lead-to-heatsink creepage: 5mm



These larger distances ensure more reliable and easier heatsink assembly, especially important for high-voltage applications.

Pin Holder Technology: Simplifying Assembly

Unlike traditional packages with exposed metal “mold ears,” Generation 2 features pin holder design, which increases creepage distance between mounting screws or clips and the exposed die pad (at drain potential), simplifying the mounting process while improving electrical isolation. The thinner gate and Kelvin pins prevent solder bridging during assembly, a common manufacturing issue that can lead to field failures.

Proven Performance in Real Applications

Solar Inverter Performance

The true test of any technology is how it performs in real-world applications. In solar PV inverters that use boost topology (which is common in MPPT stages), comparative measurements highlight the benefits of Generation 2: At a switching frequency of 60 kHz, Generation 2 runs 9°C cooler than Generation 1 during 10kW operation. When the frequency rises to 80 kHz, Generation 2 remains 13°C cooler than Generation 1. Increasing the switching frequency by 20 kHz causes only a 7°C temperature rise in Generation 2 as opposed to 11°C in Generation 1.

Half-Bridge Topology Results

Half-bridge configurations, the foundation of most power conversion stages, operate as synchronous buck converters. Generation 2 demonstrates:

- Increased efficiency across the entire operating range
- Reduced temperatures for high-side switching and low-side synchronous rectification devices

These improvements in switching and thermal performance directly result in higher system efficiencies and lower operating temperatures.

Mastering Parallel Operation: A Critical Design Challenge

Understanding the Paralleling Challenge

Paralleling SiC devices presents inherent challenges due to variations in device parameters and layout asymmetries. Three key parameters influence current sharing: Vgs threshold, the most critical for dynamic current sharing; transfer characteristic, which affects current distribution during transitions; and RDS(on), which features a positive temperature coefficient that naturally helps balance steady-state currents.

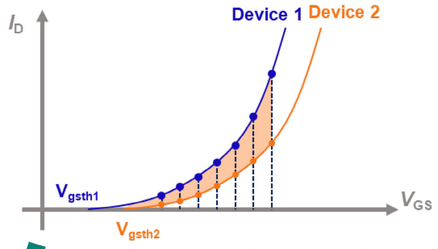
The challenge increases because the Vgs threshold has a negative temperature coefficient. When devices have mismatched thresholds, the device with the lower threshold turns on earlier, carries more current, experiences higher losses, and reaches higher temperatures. This temperature increase further lowers its threshold, creating a destructive positive feedback loop that can lead to device failure.

CoolSiC™’s Statistical Advantage

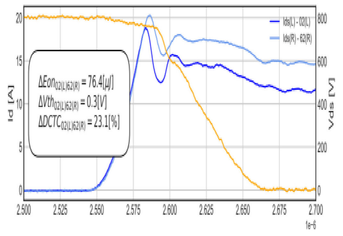
A comparative analysis of Vgs threshold distributions demonstrates CoolSiC™’s superiority. While all technologies experience some manufacturing variation, CoolSiC™ maintains tight parameter control, with most devices clustering around the typical threshold value. Other trench-based technologies exhibit wider distributions, while planar technologies show the greatest variation. This advantage stems from the trench cell design’s inherent resistance to process variations.

- Paralleling offers:
  - Enhanced power Capability
  - Optimized Cost/performance matching for system output requirement
- Parameters influencing paralleling performance:
  - $V_{GS(th)}$, Transfer Characteristics, $R_{DS(on)}$

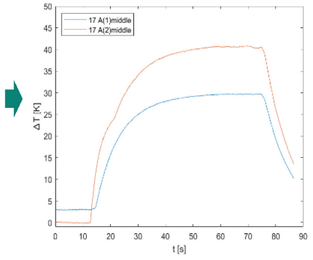
$V_{GS(th)}$ variation among paralleled devices is very critical parameter

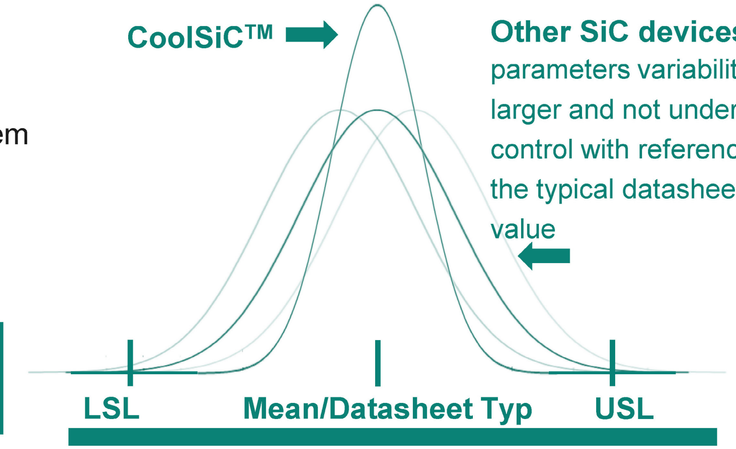


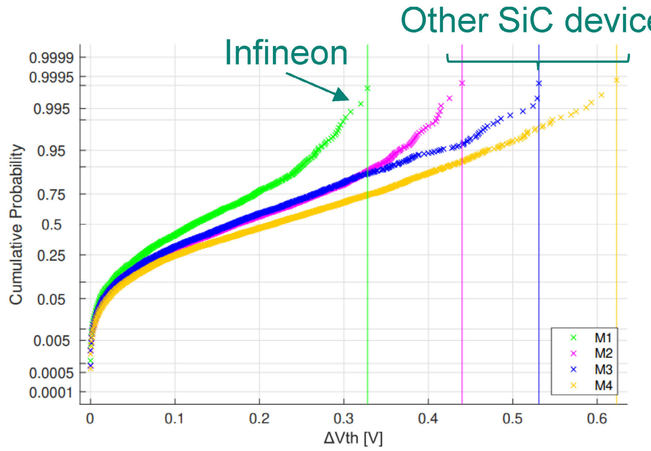
results in different E_{on}



temperature imbalance and risk of thermal instability







References:
[1] A. Piccioni, N. Seltner, T. Aichinger, B. Zippelius: „Influence of SiC MOSFET Gate Technologies on Imbalanced Performance in Hard Switching Parallel Operation"; published at the ISPSD 2024
[2] A. Piccioni, N. Seltner: „Impact of Parameter Spread in Parallel-Operated SiC MOSFETs for Hard-Switching Conversion"; published at the PCIM 2024

Thermal Balance in Parallel Operation

Apart from having a tight parameter distribution, CoolSiC™'s lower negative temperature coefficient (αVGS(th)) provides better stability. Application tests comparing parallel operation show that CoolSiC™ devices with a 9°C temperature difference outperform planar devices with a 26°C difference. This improved thermal stability reduces derating requirements and ensures more reliable parallel performance, allowing for higher power density designs.

Robustness Features: Designing for the Unexpected

200°C Overload Capability

Generation 2's ability to operate at 200°C (qualified for 100 hours) offers greater design flexibility. Since nearly every application encounters overload events, this capability provides real benefits. In UPS applications experiencing output short circuits, the 200°C rating allows for 6% higher output power. For applications with overload-limited dimensioning, this improvement compounds with electrical and thermal enhancements, reducing the cost per ampere.

Immunity to Parasitic Turn-On

While parasitic turn-on (PTO) can cause catastrophic shoot-through events in many SiC technologies, CoolSiC™ shows exceptional immunity to this phenomenon. Half-bridge testing with dV/dt rates up to 80V/ns indicates that Generation 2 can operate at much higher gate resistance values before experiencing PTO. This robustness allows operation with a 0V gate-source voltage during off-states, simplifying gate drive design without sacrificing reliability.

Short-Circuit and Avalanche Protection

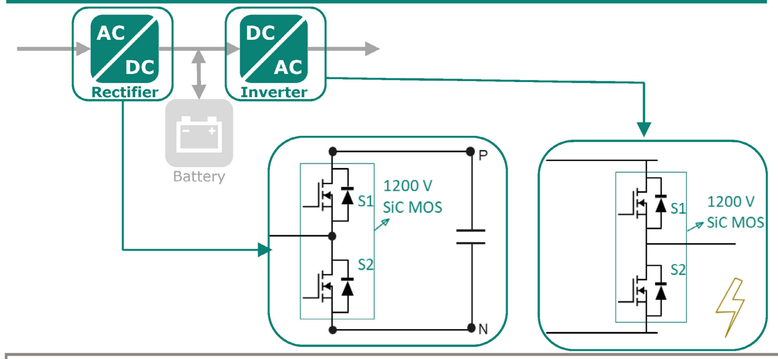
Unique among SiC technologies, CoolSiC™ provides a guaranteed short-circuit withstand capability: 2 microseconds of guaranteed withstand time (as specified in the datasheet) and a full avalanche ruggedness rating. These features improve system robustness for applications where devices might face fault conditions.

Conclusion: A Holistic Advancement

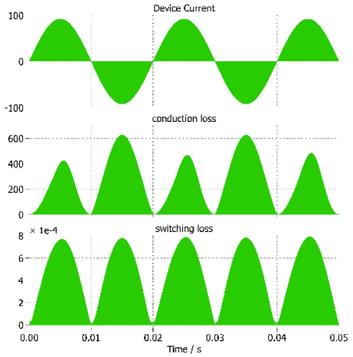
Generation 2 CoolSiC™ devices in TO247 4-pin high creepage packages provide more than just incremental improvements—they deliver comprehensive enhancements across every parameter. With a 25% reduction in switching losses, a 30% improvement in thermal resistance, better paralleling ability, and strong fault tolerance, these devices address real-world challenges while remaining easy to implement.

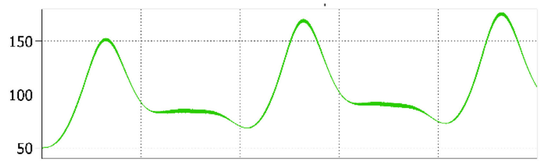
The combination of electrical performance, thermal management, innovative mechanical design, and innate robustness creates a technology platform that not only simplifies system design but also enables engineers to push the boundaries of power density and efficiency. Whether replacing existing devices or designing new systems, Generation 2 offers all the features needed for successful deployment in demanding industrial applications.

A Rectifier and Inverter stage in UPS



- **Assuming a UPS of 18.5 kW (P_{out}) rating with 26.8 Arms at full load during normal operation** (IMZC120R026M2H)
  - Current during a short circuit = 250% of UPS current rating = 67 A_{rms}
  - Overload time duration during= 50 msec
    - This leads to a Tj during overload operation = 185 °C
- The accumulated 100 h over the lifetime leads to the total number of short circuit events = **7M overload cycles!**
- !please note: DS limits ➔ up to 5000 cycles. Maximum ΔT limited to 100 K.





- **without 200 °C overload spec. ➔ T_{vjmax} = 160 °C**
  - ➔ I_{out} = 25.2 A_{rms} ➔ for T_{vj} < 175 °C during an overload condition
  - OR use a lower Rdson device to allow the same system power leading to higher BOM cost

- The 200 °C overload spec. enables 6 % increase in output power
- Transition from G1 to G2 lead to additional output power gain due to 200 °C overload spec, in addition to the electrical and thermal performance improvement

- Allow the device to survive an overload event e.g. in
  - UPS: during output short circuit
  - PV solar: during LVRT
  - Server SMPS: high pulse current (surge)
  - EV charging: during grid fluctuation/high current pulses,
- Offers higher headroom during overload event, reducing the safety margin leading to
  - **Higher output power and lower Cost/Ampere**

Chapter 3

Infineon's Top-Side Cooled (TSC) Q-DPAK Package

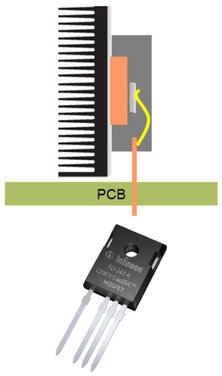
The power electronics industry has long faced a fundamental dilemma: choosing between through-hole packages for better thermal performance or surface-mount packages for easier automated assembly. Infineon's topside cool Q-DPAK package addresses this by providing both benefits in one solution.

The Evolution from Compromise to Integration

Traditional through-hole packages dominate high-power applications because they mount directly to heatsinks, offering effective thermal performance. However, this benefit comes with a cost—manual insertion and soldering processes that raise manufacturing expenses and limit scalability.

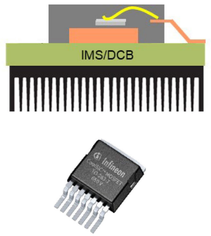
Surface-mount packages have improved manufacturing efficiency through automated assembly, especially for bottom-side cool variants. However, these packages have a weakness: heat must escape through the PCB, creating a thermal bottleneck that limits power handling capacity. The PCB itself becomes the limiting factor, preventing these devices from reaching their full potential.

The topside cool Q-DPAK package solves this issue. By allowing direct heatsink mounting, similar to a through-hole package, while maintaining surface-mount assembly compatibility, it provides excellent thermal performance without sacrificing manufacturing efficiency.



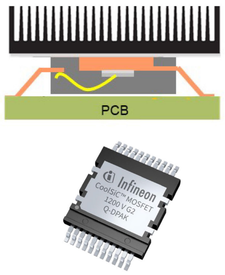
THD – Through Hole Device

- Robust thermal performance
- Manual handling
- Low pin count



SMD bottom side cooling

- Medium thermal performance
- Fully automatic handling
- High pin count



SMD top side cooling

- **Optimal** thermal performance
- **Fully automatic** handling
- **High** pin count

Engineering the Q-DPAK Architecture

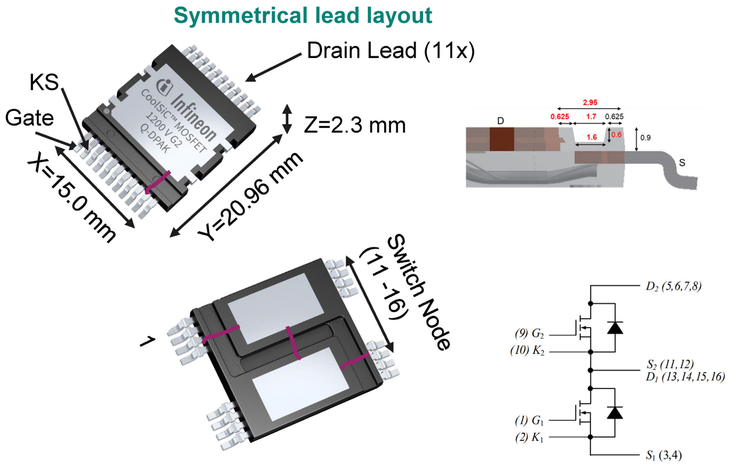
The Generation 2 Q-DPAK portfolio exemplifies how careful package design can improve performance. Available with RDS(on) values starting at 4 milliohms, these devices cover a wide range of power requirements. The package's symmetrical lead layout offers mechanical stability while supporting a larger die pad area. This larger pad serves two purposes: housing ultra-low RDS(on) dies capable of handling high currents and dispersing heat more effectively across the package surface. The increased thermal mass enhances heat dissipation directly.

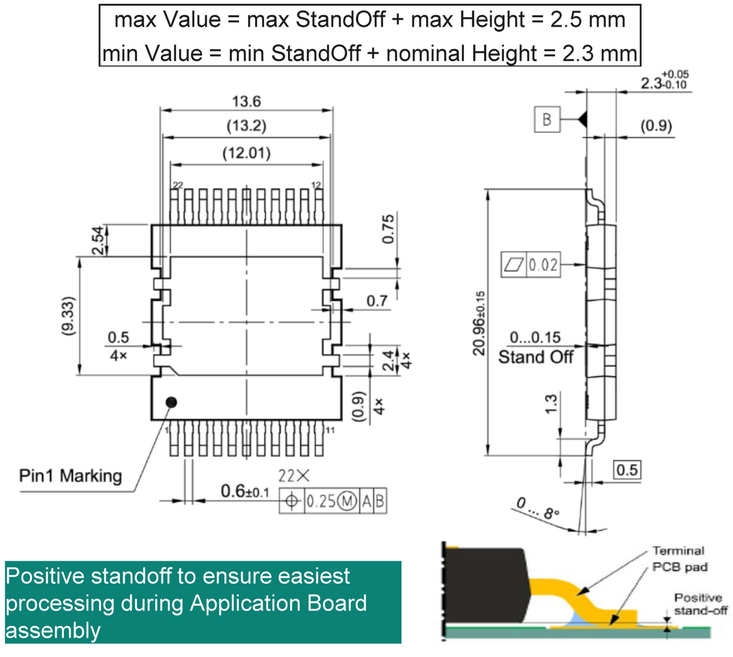
Safety considerations led to the addition of a molded groove between the die pad and the source-side lead. This feature increases the creepage distance to 4.8 millimeters—vital for high-voltage applications. Paired with Group 1 mold compound material, this extended creepage distance enables operation at RMS voltages up to 950V under Pollution Degree 2 conditions. High-voltage designers can now utilize fast-switching technology without compromising safety margins.

All Q-DPAK variants maintain a consistent height of 2.3 millimeters, whether designed as single switches or split die pad versions supporting various switch-diode combinations. This uniformity simplifies thermal solution design across different circuit topologies.

Manufacturing efficiency was also a key factor: a 150-micrometer positive standoff raises the package body above the lead edges. This elevation allows the use of standard-height stencils during reflow soldering and eliminates the need for extra board cleaning steps before component placement. What might seem like a minor detail actually streamlines the entire assembly process.

Creepage considerations HV Q-DPAK





Pollution degree	Material Group	Creepage distance	Vrms Voltage
2	1*	4.8mm	950 V

Positive standoff to ensure easiest processing during Application Board assembly

Unlocking Switching Performance

The topside cool architecture allows significant improvements in circuit layout that directly boost electrical performance. In bottom-side cool packages, the current return path must go around the device laterally, forming a large loop with parasitic inductance. This inductance limits switching speed and causes voltage overshoots that stress components and create electromagnetic interference.

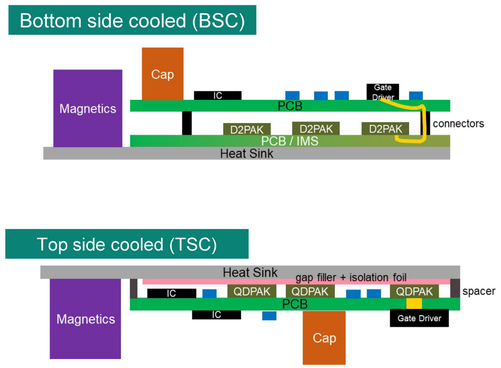
The Q-DPAK package allows the current return path to run directly beneath the device. This placement creates opposing magnetic fields that cancel each other out, reducing loop inductance. Lower inductance results in faster switching transitions with less overshoot and ringing—exactly what's needed to unlock the potential of wide-bandgap semiconductors.

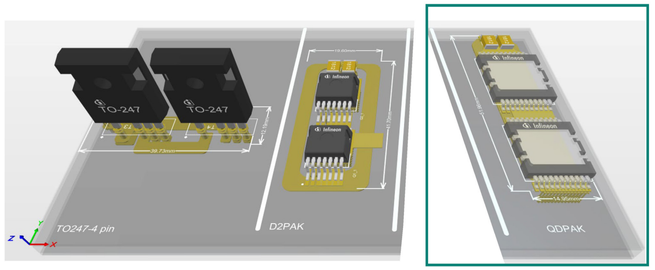
This layout optimization extends beyond the power loop. Topside cooling effectively doubles the usable PCB area compared to bottom-side cooled packages, eliminating the need for insulated metal substrate boards. All components can be mounted on standard FR4 PCBs with tighter spacing, further optimizing both the commutation loops and gate drive paths.

Quantifying the Electrical Benefits

The significance of optimized package design becomes apparent when evaluating actual device performance. Testing 1200 V Generation 2 CoolSiC™ devices illustrates how packaging directly influences switching behavior.

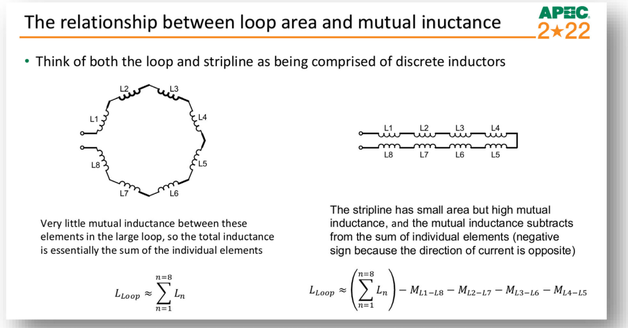
Comparing devices with identical RDS(on) values in Q-DPAK versus TO-247 packages under the same circuit conditions reveals differences. The Q-DPAK enables faster dV/dt and dI/dt transitions—the key indicators of efficient switching. These faster transitions directly result in reduced switching losses, with measurements showing a 39% reduction in combined turn-on and turn-off energy losses.





TOP SIDE COOLED (TSC):

- Optimized cooling and system level costdown
- Enable to minimize power loop inductance
- Simplify system layout, reducing complexity / time-to-market



[Eric Persson, "PCB Layout Techniques for Optimizing Performance of Surface-Mounted Wide BanDgap Power Electronic Circuits", Professional Educational Seminar, APEC 2022]

This improvement results from eliminating the parasitic inductances found in TO-247 packages. Although TO packages limit switching speed because of their physical design, Q-DPAK packages eliminate these restrictions, allowing silicon carbide technology to fully realize its performance advantages.

Building a Comprehensive Platform

The benefits extend beyond individual devices through Infineon's x-DPAK platform. By standardizing on consistent package heights, designers can integrate different technologies—CoolMOS, IGBTs, CoolGaN, and CoolSiC™—on a single PCB under one heatsink.

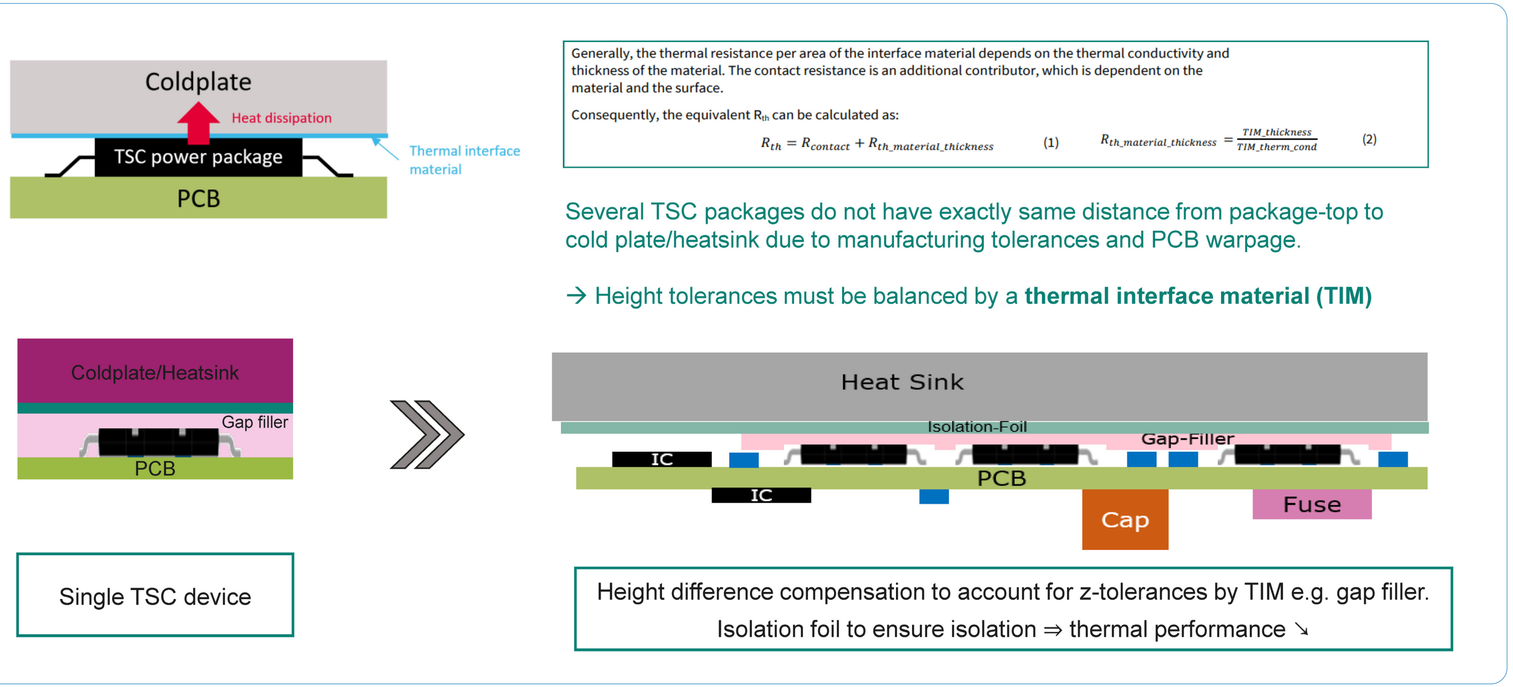
This flexibility enables optimization of each circuit function without mechanical limitations. The platform scales from compact, low-power devices to large-die, high-current IGBTs, all within the same mechanical framework. Circuit designers can select the best technology for each function while maintaining assembly compatibility.

JEDEC registration promotes industry-wide standardization, supporting second-source options and encouraging widespread adoption. Available configurations include Q-DPAK dual variants for half-bridge topologies (with matched switches), boost topologies (switch plus diode), bridge rectifiers (dual CoolSiCTM diode), and Q-DPAK mono versions for single-switch applications.

Addressing the Assembly Challenge

The direct heatsink mounting that improves thermal performance also presents assembly challenges that must be carefully managed. Unlike bottom-side cool packages, which rely on PCB mounting, topside cool packages require precise control of the thermal interface between the device and heatsink.

Package height tolerances, though tightly controlled, still need to be accommodated with thermal interface materials. When multiple devices are mounted under a single heatsink, ensuring uniform contact across all devices becomes essential for balanced thermal performance and reliability.



System designers must consider multiple factors: package height variations, potential PCB warpage under mounting pressure, electrical isolation requirements, and mechanical assembly constraints. Each application requires careful evaluation to optimize the thermal solution.

Thermal Interface Solutions

Gap Pad Approach

Compressible gap pads provide one approach to address height tolerance challenges. Made of solid materials, they come in various thicknesses and thermal conductivities, providing design flexibility. Testing with a gap pad that has a thermal conductivity of 6 W/m·K, initially 1 millimeter thick and compressed to 0.5 millimeters with mechanical standoffs, showed a thermal resistance of 1 C/W.

Reducing standoff height can improve thermal performance by decreasing the thermal interface thickness. However, this also increases mechanical stress on the PCB, which could cause warping and impact long-term reliability. Softer materials can withstand higher mounting pressures while reducing stress, but typically have lower thermal conductivity. Engineers must balance thermal efficiency with mechanical reliability for each specific application.

Ceramic Substrate Method

For applications that require electrical isolation along with good thermal performance, aluminum oxide ceramic substrates provide a practical alternative. With a thermal conductivity of around 30 W/m·K, ceramics outperform polymer-based options. Testing involved a 1.5-millimeter ceramic with 50-micrometer layers of thermal grease on both sides.

Comparative measurements between Q-DPAK and TO-247 packages using identical chip sizes and thermal stacks produced similar results, both around 1.2 C/W in thermal resistance. However, this method is limited to a few devices per heatsink, since Q-DPAK height tolerances usually require gap-filling materials thicker than the 50-micrometer grease layers needed for multi-device assemblies.

Liquid Gap Filler Systems

Complex assemblies with multiple devices benefit from liquid gap filler materials combined with isolation foils. The liquid material naturally conforms to height variations while providing electrical isolation. Automated dispensing equipment can apply these materials efficiently, supporting high-volume manufacturing.

The additional isolation layer does impact thermal performance, but careful material selection minimizes this penalty. As with all thermal interface options, the overall stack's thermal conductivity determines the achievable thermal resistance.

Implementing Topside Cool Technology

Success with topside cool packages depends on understanding both their benefits and assembly needs. These packages deliver on their promise of combining thermal performance with automated assembly, but achieving the best results requires careful attention to thermal interface design.

Infineon offers comprehensive design tools and resources to support implementation, helping designers select thermal interfaces and optimize assembly. When properly implemented, topside cool Q-DPAK packages enable power electronic systems that are both thermally efficient and cost-effective to produce, finally addressing the industry's longstanding trade-off between performance and manufacturing efficiency.

Chapter 4

Infineon Tools and Resources for Device Simulation and Design

Designing with power semiconductors demands accurate simulation and tested reference implementations. Infineon provides both through a complete ecosystem that includes basic device models and full system demonstrations.

The Simulation Challenge: From Basic Models to Real-World Performance

Engineers begin their design process with simulation, and Infineon provides both PLECs and SPICE simulation models for all discrete devices. These models are compatible with offline simulators, forming the foundation of the design workflow. However, basic models alone cannot fully capture the complexity of real applications.

IPOSIM, Infineon's online simulation tool, closes this gap. It allows you to simulate how the device performs within various application circuits, helping assess performance across different topologies. The tool provides design data by calculating switching and conduction losses, along with the device's thermal behavior. This insight helps in selecting the right product for specific application conditions. Additionally, engineers can compare the performance of multiple products under different input requirements, making the selection process easier.

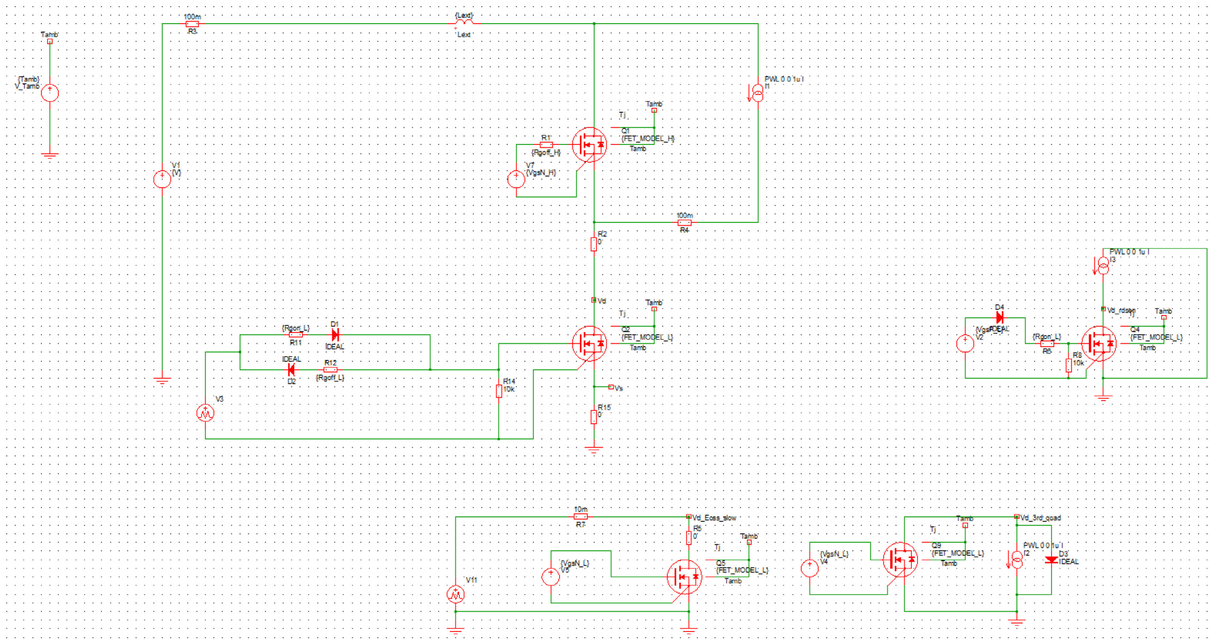
The Reality Gap: Why Standard Models Fall Short

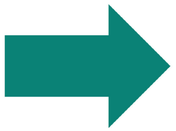
Traditional simulation often encounters a key challenge: predefined PLECs models depend on lookup tables for device losses, making it hard to account for changing board conditions or gate driving scenarios. Since device performance is influenced by these external circuit factors, this limitation can affect accuracy.

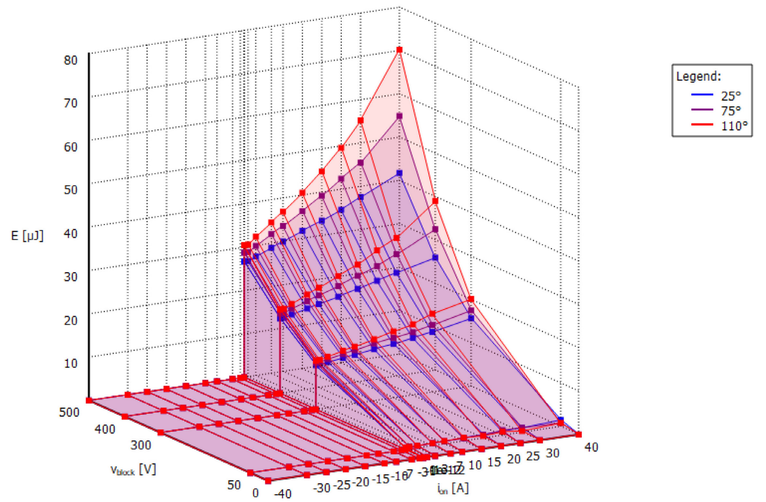
IPOSIM's new SPICE-in-loop simulation feature directly tackles this issue. It allows users to develop custom PLECs models tailored to their specific gate driving conditions or board stray inductances. The feature generates a PLECs XML file from a SPICE circuit and performs steady-state simulations for any application scenario. This new capability enables precise simulation of these behaviors and effects, reducing the gap between idealized models and real-world circuit performance.

From Simulation to Implementation: Q-DPAK Reference Designs

While simulation tools predict performance, reference designs verify it. Infineon will soon release Q-DPAK reference designs that serve as resources for system designers, demonstrating how simulation results translate into real hardware.






E [µJ]
80
70
60
50
40
30
20
10
500
400
300
V_{block} [V]
50
0
-40
-30
-25
-20
-15
-10
10
15
20
25
30
40
i_{on} [A]
Legend:
25°
75°
110°

High-Power Solar and Energy Storage Design

The reference design features a 3-level NPC2 topology capable of handling 10 kilowatts of power. Operating bidirectionally with a target efficiency of over 99%, this design is ideal for solar and energy storage applications. The implementation includes design elements: CoolSiC™ Generation 2 devices in Q-DPAK packages, a 2-level slew rate control EiceDRIVER from Infineon, and appropriate thermal assembly for the Q-DPAK. This design provides a solution to integrate the inverter in solar and energy storage systems, delivering both high performance and high power density, and confirming the predictions made by simulation tools.

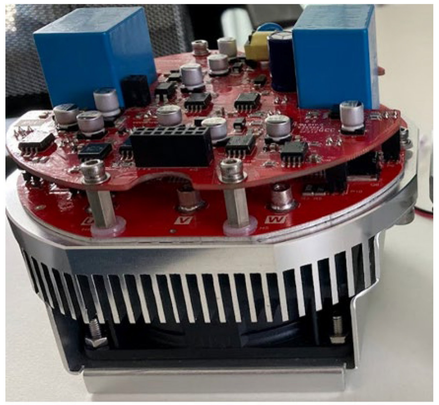
Servo Motor Drive Implementation

Another reference board showcases Q-DPAK half-bridge switches in a servo motor drive inverter board. Compared to board designs that use devices cooled from the bottom side, the Q-DPAK offers higher power density, which is beneficial in space-limited industrial settings.

Standard cooling assembly

Stack: FR4 + IMS +

- IMS board used for power components
- FR4 PCB used for IC/driver/magnetics components



Top-side cooling assembly

Stack: FR4 +

- Single FR4 PCB used on both sides for **all** components, no IMS board needed
- Reduced stray inductance

Your Complete Design Journey

To help you start using these tools and turn simulations into successful designs, Infineon offers additional resources:

For understanding the technology: Application pages and product web pages featuring:

- Application notes on Gen 2 technology
- Heat sink assembly guidelines for the Q-DPAK
- Short videos explaining some technical features of the product

For detailed Implementation:

- Complete reference design documentation
- Thermal assembly guidelines
- Circuit optimization techniques

These resources connect the simulation environment to real-world applications, supporting your journey from concept to production at every step. For more detailed information, please visit the resources available on Infineon's website.

A New Era in Power System Design

The power electronics industry is at a critical turning point, and Infineon's CoolSiC™ technology portfolio offers the comprehensive solutions engineers need to face future challenges now. From the robust trench-based architecture and Generation 2 performance improvements to innovative packaging options like the TO-247-4HC and topside-cooled Q-DPAK, this technology platform eliminates traditional design trade-offs while delivering significant improvements in efficiency, thermal management, and power density. When combined with advanced simulation tools and validated reference designs, CoolSiC™ technology not only enables better power systems but also fundamentally expands the possibilities in power electronics design, empowering engineers to create compact, high-efficiency solutions that shape the future of industrial applications.

Semiconductors are crucial to solve the energy challenges of our time and shape the digital transformation. This is why Infineon is committed to actively driving decarbonization and digitalization. As a global semiconductor leader in power systems and IoT, we enable game-changing solutions for green and efficient energy, clean and safe mobility, as well as smart and secure IoT. We make life easier, safer, and greener. Together with our customers and partners.
For a better tomorrow.

Mouser Electronics is an authorized semiconductor and electronic component distributor focused on New Product Introductions from its leading manufacturer partners. Serving the global electronic design engineer and buyer community, the global distributor's website, www.mouser.com, is available in multiple languages and currencies and features more than 6.8 million products from over 1,200 manufacturer brands. Mouser offers 28 support locations worldwide to provide best-in-class customer service in local language, currency and time zone. The distributor ships to over 650,000 customers in 223 countries/territories from its 1 million-square-foot, state-of-the-art distribution facilities in the Dallas, Texas, metro area. For more information, visit www.mouser.com.